

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket: NL 030336
ANDREA GIRALDO ET AL.	Group Art Unit: 2629
Serial No.: 10/551,023	Examiner: JENNIFER L. ZUBAJLO
Filed: SEPTEMBER 29, 2005	CONF. NO.: 8259
TITLE: DISPLAY DEVICE	

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Appellants herewith respectfully present its Brief on Appeal
as follows:

REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA.

RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge and belief, there are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-14 are pending in this application. Claims 1-14 are rejected in the Final Office Action that issued December 27, 2007. This rejection was upheld, in an Advisory Action that issued March 17, 2008. Claims 1-14 are the subject of this appeal.

STATUS OF AMENDMENTS

An Amendment After Final Action was filed February 26, 2008 in response to a Final Office Action that issued December 27, 2007. An Advisory Action of March 17, 2008 considered the Amendment After Final Action however, upheld the rejections contained in the Final Office Action. This Appeal Brief is in response to the Final Office Action that rejected Claims 1-14 and the Advisory Action that upheld those rejections.

SUMMARY OF CLAIMED SUBJECT MATTER

It should be explicitly noted that it is not the Appellants' intention that the currently claimed method be limited to operation within this illustrative devices and method described below beyond what is required by the claim language. Further description of the illustrative devices and method is provided indicating portions of the claims which cover the illustrative devices and method merely for compliance with requirements of this appeal without intending any further interpreted limitations be read into the claims as presented.

The present invention, for example as claimed in claim 1, relates to a display device including a display (e.g., see, FIGS. 1, 2; display 2 and accompanying description contained on page 5, lines 3-6) with a plurality of light emitting elements (e.g., see, FIGS. 1, 2, 5; display pixels 3 and LED in FIG. 5), and data lines (e.g., see, FIGS. 2, 5, data lines 13, selection lines 12; and the accompanying description contained on page 6, lines 5-8) for providing pulse width modulation signals to the light emitting elements (e.g., see, page 6, lines 16-22). Means (e.g., see, FIG. 2 and accompanying description on page 5, lines 5-12, with

corresponding structure illustratively provided by control unit 10 coupled to data driver 8 and row selection 7; additional illustrative structure is shown in FIGs. 5, 8 including transistors T1, T2 and capacitor C; see, accompanying description on page 6, lines 5-16 and page 7, lines 18-30; additional illustrative structure is shown in FIG. 10, including transistors T0, T3, T4, T11 and capacitor C; see, accompanying description on page 8, lines 15-23; additional illustrative structure is shown in FIG. 11, including independent current sources I1, I2, switch transistors S1, S2, transistors T3, T4, T11, capacitor C and dumping unit 19; see, accompanying description on page 9, lines 1-17) are coupled to the data lines 13 (e.g., see, data driver 8 is coupled to the data lines 13; row selection 7 is coupled to the selection lines 12) for generating, during time intervals of a frame period (e.g., see, page 6, lines 16-24), at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals (e.g., see, FIGs. 5-9, and particularly time intervals SF1, SF2 in FIGs. 6, 7 and 9), wherein the generating means (e.g., see, control unit 10 supplies current I1, I2 over

lines 18; page 9, lines 1-7) generates the first and second time intervals in an order that reduces dead times between the time intervals (e.g., see, page 7, lines 2-4 and page 9, lines 7-9).

The present invention, for example as claimed in claim 11, relates to a method for driving a display device including a display (e.g., see, FIGs. 1, 2; display 2 and accompanying description contained on page 5, lines 3-6) with a plurality of light emitting elements (e.g., see, FIGs. 1, 2, 5; display pixels 3 and LED in FIG. 5) and data lines coupled to the light emitting elements (e.g., see, FIGs. 2, 5, data lines 13, selection lines 12; and the accompanying description contained on page 6, lines 5-8). The method includes providing pulse width modulation signals to the data lines (e.g., see, page 6, lines 16-22) and generating in synchronization with the pulse width modulation signals, during time intervals of a frame period (e.g., see, page 6, lines 16-24), at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals (e.g., see, FIGs. 5-9, and particularly time intervals SF1, SF2 in FIGs. 6, 7 and 9). The first and second time intervals are

generated in an order that reduces dead times between the time intervals (e.g., see, page 7, lines 2-4 and page 9, lines 7-9).

The present invention, for example as claimed in claim 12, relates to a display device including a display (e.g., see, FIGs. 1, 2; display 2 and accompanying description contained on page 5, lines 3-6) with a plurality of light emitting elements (e.g., see, FIGs. 1, 2, 5; display pixels 3 and LED in FIG. 5), and data lines (e.g., see, FIGs. 2, 5, data lines 13, selection lines 12; and the accompanying description contained on page 6, lines 5-8) for providing pulse width modulation signals to the light emitting elements (e.g., see, page 6, lines 16-22). A controller (e.g., see, FIG. 2 and accompanying description on page 5, lines 5-12, control unit 10 coupled to data driver 8 and row selection 7; FIGs. 5, 8 including transistors T1, T2 and capacitor C; see, accompanying description on page 6, lines 5-16 and page 7, lines 18-30; FIG. 10, including transistors T0, T3, T4, T11 and capacitor C; see, accompanying description on page 8, lines 15-23; FIG. 11, including independent current sources I1, I2, switch transistors S1, S2, transistors T3, T4, T11, capacitor C and dumping unit 19; see, accompanying description on page 9, lines 1-17) is configured

to generate, during time intervals of a frame period (e.g., see, page 6, lines 16-24), at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals (e.g., see, FIGs. 5-9, and particularly time intervals SF1, SF2 in FIGs. 6, 7 and 9). The controller is configured to generate the time intervals in an order that reduces dead times between the time intervals (e.g., see, page 7, lines 2-4 and page 9, lines 7-9).

GROUND'S OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-5 and 9-14 of U.S. Patent Application Serial No. 10/551,023 are obvious under 35 U.S.C. §103(a) in light of U.S. Patent No. 5,652,600 to Khormaei ("Khormaei") in view of allegedly Applicant's Admitted Prior Art (AAPA); whether claims 6 and 7 of U.S. Patent Application Serial No. 10/551,023 are obvious under 35 U.S.C. §103(a) over Khormaei in view of allegedly AAPA in further view of U.S. Patent No. 6,567,171 to Rushing ("Rushing"); and whether claim 8 of U.S. Patent Application Serial No. 10/551,023 is obvious under 35 U.S.C. §103(a) over Khormaei in view of allegedly AAPA in further view of U.S. Patent No. 4,771,278 to Pooley ("Pooley"). The Appellants respectfully wish the Board to address the patentability of independent claims 1, 11 and 12, and further claims 2-10 and 13-14 as respectively depending on one of claims 1 and 12, based on the requirements of claims 1, 11 and 12. This position is provided for the specific and stated purpose of simplifying the current issue on appeal. However, the Appellants herein specifically wish to reserve the right to argue and address the patentability of each of the further claims at a later date should the separately patentable subject matter of those claims

later become an issue. Accordingly, this limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of claims 1, 11 and 12, is not intended as a waiver of Appellants' right to argue the patentability of the further claims and claim elements at that later time.

ARGUMENT

Claims 1-5 and 9-14 are said to be unpatentable over Khormaei in view of allegedly AAPA; claims 6 and 7 are said to be unpatentable over Khormaei in view of allegedly AAPA in further view Rushing; and claim 8 is said to be unpatentable over Khormaei in view of allegedly AAPA in further view of Pooley.

\$103(a) Rejection of Claims 1-5 and 9-14 over Khormaei in view of AAPA

1. Khormaei

It is undisputed that Khormaei does not show "the generating means generates the first and second time intervals in an order that reduces dead times between the time intervals." (See, Final Office Action, page 3, first paragraph.)

2. AAPA

The Final Office Action relies on AAPA for showing "the generating means/controller generates the first and second time intervals in an order that reduces dead times between the time intervals" and cites FIGs. 3, 4 and paragraphs [0005], [0037],

[0039] for showing this element but it is respectfully submitted that reliance on AAPA is misplaced.

While it is true that FIGs. 3, 4 show schematical timing diagrams according to the prior art, FIGs. 3 and 4 show the first and second time intervals generated in a sequential order (e.g., SF1, SF2, SF3) and not in an order that reduces dead times between the time intervals. Paragraph [0005] does state that "[i]n an MLA scheme, dead times between the subfields are minimized by proper algorithms" but does not disclose or suggest an ordering that reduces dead times between the time intervals. Paragraph [0037] describes FIG. 3 which shows a timing diagram illustrative of pulse width modulation (PWM) wherein the time intervals are sequentially ordered. Nowhere within paragraph [0037] is it disclosed or suggested that an ordering would be other than sequential and it certainly is not disclosed or suggested that an ordering may be provided that reduces dead times between the time intervals.

Paragraph [0039] describes FIG. 4 which shows a timing diagram illustrative of employing multiline row addressing (MLA) in combination with PWM again where the time intervals are sequentially ordered. While paragraph [0039] does state that "it

may be preferred to shuffle or mix up the time intervals within the frame period in order to obtain the most efficient result", this is not disclosed in the present patent application as being in the prior art with regard to FIG. 4.

The Advisory Action in a response to Arguments section starting on page 2 and ending in the first paragraph on page 3, does little more than restate the same arguments discussed above regarding the Final Office Action. Specifically, the Advisory Action takes the position that page 5, lines 31-34 (stated as paragraph [0005] from the publication) together with FIGs. 3 and 4 shows "the first and second time intervals are generated in an order that reduces dead times between the time intervals" as recited in claim 11 and as substantially recited in each of claims 1 and 12.

It is again respectfully submitted that this position is not supported by the cited figures or portions of the present patent application as discussed in detail above. FIGs. 3 and 4 show a sequential ordering. As stated on page 5, lines 32-34 of the present application, (emphasis added) "[a]s can be clearly observed [in FIG. 4], in MLA the amount of dead times between the time

intervals SF and for the rows 4 is variable and can be minimized by applying proper algorithms." Yet FIG. 4 show a sequential ordering and not first and second time intervals generated in an order that reduces dead times between the time intervals as suggested by the Final Office Action and the Advisory Action. Since FIG. 4 does not show other than a sequential ordering and the cited portion of the present patent application stipulates that FIG. 4 shows minimizing dead times "by applying proper algorithms", how can the application of these prior art "proper algorithms" result in other than the sequential ordering shown in FIG. 4? Where does the Final Office Action and the Advisory Action come to the teaching of an ordering that reduces dead times when this is nether shown in the AAPA figures nor described in the specification regarding AAPA.

It is respectfully submitted that the only suggestion of the ordering to reduce dead times is provided in the description of the present patent application, for example as provided on page 7, lines 2-4 and page 9, lines 7-9. By the stated "broadly interpreted" position provided in the Response to Arguments section of the Advisory Action, would any system of reducing dead times between time intervals be similarly obvious since "proper

algorithms" are suggested? This is an untenable position to maintain that a teaching of an ordering to reduce dead times is rendered obvious by a general stipulation of proper algorithms regarding a figure, namely FIG. 4, which shows no such ordering to reduce dead times.

The Appellants can find no place where the "ordering" substantially recited in each of claims 1, 11 and 12 can be found or is suggested other than in the description of the present invention and as clear, the Final Office Action and Advisory Action may not utilize the teaching of the present patent application regarding the present invention, as the suggestion for this feature with regard to the prior art.

The Appellants further maintain that FIGs. 3 and 4 do not show a multilevel power addressing scheme wherein during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals as substantially recited in claims 1, 11 and 12. While Khormaei is cited for showing this element, it is respectfully submitted that Khormaei is merely a prior art reference that

utilizes time intervals of the frame period that have a binary weighted distribution (see, paragraph [0037] of the present application. However, in the present invention, a first non-zero emission level of a light emitting element is applied during a first one of the time intervals and a second non-zero emission level is applied during a second one of the time intervals instead of only once as taught by Khormaei and AAPA.

The Advisory Action, on page 3, numbered paragraph 3, states that the Arguments contained in the Amendment After Final Office Action on this point where directed to elements not recited in the rejected claims. This position is respectfully refuted. The comments addressed in the Amendment After Final Office Action referred to a section of the specification (see, page 6, lines 27-29) which states that in the MPA-approach the individual time intervals SF are in fact used n times instead of only once. As a result the number of bits for gray scale levels is best enhanced by a factor of n. Claims 1, 11 and 12 substantially recite "at least a first non-zero emission level ... and a second non-zero emission level" in which case "n" is at least "two" and the grey scale

levels therefore are enhanced by a factor of "2" instead of only "1" (namely, no enhancement) as taught by Khormaei and AAPA.

Accordingly, it is respectfully submitted that the device of claim 1 is not anticipated or made obvious by the teachings of Khormaei in view of AAPA. For example, Khormaei in view of AAPA does not disclose or suggest, a device that amongst other patentable elements, comprises (illustrative emphasis provided) "means coupled to the data lines for generating, during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the generating means generates the first and second time intervals in an order that reduces dead times between the time intervals" as recited in claim 1.

Further, it is respectfully submitted that the method of claim 11 is not anticipated or made obvious by the teachings of Khormaei in view of AAPA. For example, Khormaei in view of AAPA does not disclose or suggest, a method that amongst other patentable elements, comprises (illustrative emphasis provided) "generating in synchronization with the pulse width modulation signals, during

time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the first and second time intervals are generated in an order that reduces dead times between the time intervals" as recited in claim 11.

Further still, it is respectfully submitted that the device of claim 12 is not anticipated or made obvious by the teachings of Khormaei in view of AAPA. For example, Khormaei in view of AAPA does not disclose or suggest, a device that amongst other patentable elements, comprises (illustrative emphasis provided) "a controller configured to generate, during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the controller is configured to generate the time intervals in an order that reduces dead times between the time intervals" as recited in claim 12.

Based on the foregoing, it is respectfully submitted that claims 1, 11 and 12 are patentable over Khormaei in view of AAPA.

Claims 2-5, 9-10 and 13-14 respectively depend from one of claims 1 and 12 and accordingly are allowable for at least this reason as well as for the separately patentable elements contained in each of the claims.

§103(a) Rejection of Claims 6-7 over Khormaei in view of AAPA in further view of Rushing

1. Rushing

Rushing is cited for allegedly showing elements of the dependent claims 6 and 7 yet does nothing to cure the deficiencies in Khormaei in view of AAPA.

Claims 6 and 7 each depend from claim 1 and accordingly are allowable based at least on the allowability of claim 1 as well as for the separately patentable elements contained in each of claims 6-7.

§103(a) Rejection of Claim 8 over Khormaei in view of AAPA in
further view of Pooley

1. Rushing

Pooley is cited for allegedly showing elements of the dependent claim 8 yet does nothing to cure the deficiencies in Khormaei in view of AAPA.

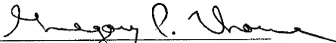
Claim 8 depends from claim 1 and accordingly is allowable based at least on the allowability of claim 1 as well as for the separately patentable elements contained in claim 8.

CONCLUSION

Claims 1-14 are patentable over Khormaei in view of AAPA alone and in view of Rushing and Pooley. Thus the Examiner's rejection of claims 1-14 should be reversed.

Based on the above arguments, Appellants respectfully submit that the subject invention is not anticipated or rendered obvious by the prior art and is patentable thereover. Therefore, Appellants respectfully request that this Board reverse the decisions of the Examiner in rejecting claims 1-14 and allow this application to pass on to issue.

Respectfully submitted,

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APPENDIX A

CLAIMS ON APPEAL

1. A display device comprising:

a display with a plurality of light emitting elements, and data lines for providing pulse width modulation signals to the light emitting elements; and

means coupled to the data lines for generating, during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the generating means generates the first and second time intervals in an order that reduces dead times between the time intervals.

2. The display device according to claim 1, wherein the display further comprises selection lines, each selection line being coupled to a part of the plurality of light emitting elements, the generating means being further coupled to the selection lines for applying a multiline addressing scheme to the data lines and the selection lines.

3. The display device according to claim 1, wherein the generating means are adapted to generate time intervals of a substantially binary weighted duration wherein each of the time intervals is assigned the substantially binary weighted duration regardless of emission levels during each of the time intervals.
4. The display device according to claim 1, wherein the generating means are adapted to generate time intervals of a substantially binary weighted duration regardless of an ordering of the time intervals.
5. The display device according to claim 1, wherein the generating means are adapted to generate the first and second emission level via the data lines in an intermixed mode.
6. The display device according to claim 3, wherein the generating means comprise a control unit, and a data driver comprising a first current source for generating the first emission

level and a second current source for generating the second emission level.

7. The display device according to claim 5, wherein the generating means are adapted to pre-charge the data lines before coupling one of the current sources to one of the data lines.

8. The display device according to claim 1, further comprising a power line for coupling a first supply voltage to the plurality of light emitting elements for generating the first emission level and a second supply voltage for generating the second emission level, respectively.

9. The display device according to claim 1, wherein the generating means are adapted to generate the second emission level at a level substantially equal to the first emission level multiplied by a number of selectable combinations of time intervals.

10. Electric device comprising a display device according to claim

1.

11. A method for driving a display device comprising a display with a plurality of light emitting elements and data lines coupled to the light emitting elements, the method comprising the steps of:

providing pulse width modulation signals to the data lines;

and

generating in synchronization with the pulse width modulation signals, during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the first and second time intervals are generated in an order that reduces dead times between the time intervals.

12. A display device comprising:

a display with a plurality of light emitting elements, and data lines for providing pulse width modulation signals to the light emitting elements; and

a controller configured to generate, during time intervals of a frame period, at least a first non-zero emission level of a light emitting element during a first one of the time intervals and a second non-zero emission level during a second one of the time intervals, wherein the controller is configured to generate the time intervals in an order that reduces dead times between the time intervals.

13. The display device according to claim 12, wherein the controller is configured to generate time intervals of a substantially binary weighted duration, wherein each of the time intervals is assigned the substantially binary weighted duration, regardless of emission levels during each of the time intervals.

14. The display device according to claim 12, wherein the controller is configured to generate time intervals of a substantially binary weighted duration regardless of an ordering of the time intervals.

Patent
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Amendment in Reply to Final Office Action of December 27, 2008
and Advisory Action of March 17, 2008

APPENDIX B

Evidence on Appeal

None

Patent
Serial No. 10/551,023
Amendment in Reply to Final Office Action of December 27, 2008
and Advisory Action of March 17, 2008

APPENDIX C

Related Proceedings of Appeal

None